Embedded Capacitors in the Next Generation Processor

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Abstract

Embedded passives technology has been of interest to electronic package designers for performance improvement and package size reduction. With the explosion of mobile phones, tablets and other hand held devices, the need for smaller form factor products with equivalent or better electrical performance makes a very compelling case for embedding passives. The benefits of embedded passives are not limited to small form factor devices. Larger die and server products requiring high performance power delivery solutions can also benefit substantially from embedded capacitors. Intel in collaboration with its suppliers has developed and commercialized a disruptive embedded capacitor technology that provides significant power delivery benefits for high performance computer applications. This is the first commercialized embedded capacitor technology used by Intel.

Introduction

Capacitors are the most commonly used passive components in electronic packaging. For microprocessor applications, capacitors are used to reduce package electrical impedance and enable the system to maintain a near-constant voltage across all operating frequencies. As of today, the majority of package capacitors are discrete components that directly mount on the surface of the substrate, module or motherboard. Figure 1 shows an example of various capacitor components and their locations in a typical package. On the substrate, capacitors are attached on the land side under the die shadow (land-side capacitor: LSC) or adjacent to the die side (die-side capacitor: DSC), where they are used for the reduction of the impedance at high frequency. These capacitors are typically $BaTiO_3$ ceramic dielectric layer based multi-layer ceramic capacitors (MLCC), which have the benefits of high reliability, small form factor and low impedance characteristics. In addition to the electrical performance need, the LSC and DSC form factors are chosen based on the die thickness, substrate ball collapse height, and substrate size. The bulk and mother board capacitors provide mid-frequency decoupling solutions, and they are typically either MLCC or electrolytic (tantalum or aluminum) for higher capacitance.

To meet increased power delivery demands, the capacitor industry is investigating further reduction in capacitor dimensions. However, this leads to multiple challenges including the handing and assembly of small form factor capacitors, dielectric degradation of finer $BaTiO_3$ grains, and reduced capacitor reliability by thinning dielectric layers [1].

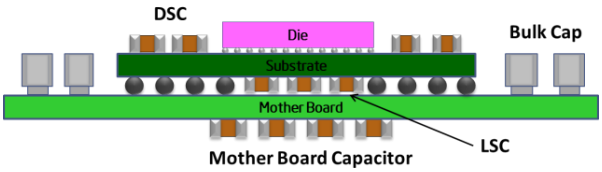

Figure 1. Schematic of various capacitor components and their locations in a typical package on the motherboard

Another approach is the use of embedded technology that has been of interest to electronic package designers for performance improvement and package size reduction. The need for smaller form factor products with equivalent or better electrical performance makes embedding passives technology very attractive. It has been reported that ultra-low profile, multi-layer ceramic capacitors have been embedded into the substrates of a variety of electronic packages, and Figure 2 shows a schematic example of embedded capacitors [2]. By embedding the capacitor into the printed circuit board core, the package footprint can be significantly reduced compared to the package mounted capacitors. In addition to the package form factor reduction, the embedded capacitor can be located under the die shadow and directly connected through multiple via-holes. This reduces the current path and package inductance, thus, it improves power delivery performance.

The benefit of embedded capacitors is not limited to the size reduction of small form factor devices. Larger die and server products requiring high performance power delivery solutions can also benefit substantially from embedded capacitors [3]. Reducing the inductance of the package capacitors (L_{PKG}) can be an effective way to improve high frequency performance. However, this is hard to accomplish with traditional decoupling options utilizing discrete capacitors because the package itself contributes significantly to this inductance. In addition, in many cases a significant portion of the die in these advanced microprocessors now sits outside the socket cavity, and thus does not have a low inductance path to LSCs. Therefore, embedding ultra-low inductance capacitors under the die shadow can dramatically improve the high frequency performance of the power delivery network.

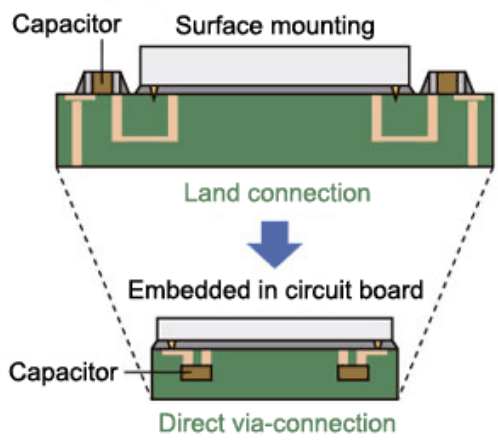

Figure 2. Example of embedded capacitors: A capacitor is embedded in a printed circuit board and it is connected through a via-hole to a semiconductor chip that is arranged right above the capacitor. This structure can significantly reduce the footprint compared with the existing surface mounting method [2].

Recently, Intel in collaboration with its suppliers has developed and commercialized a disruptive embedded capacitor technology that provides significant power delivery benefits for high performance computer applications. The schematic cross-sectional view of embedded capacitors inside the package is shown in Figure 3. The ultra-low inductance embeddable capacitor is placed under the die shadow to reduce the path to the die.

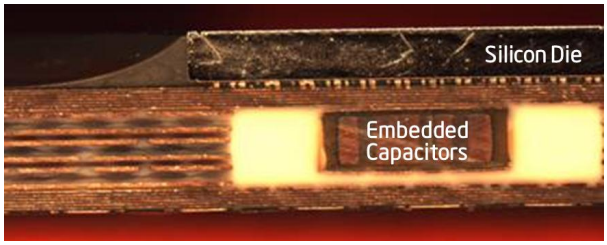

Figure 3. The schematic cross-sectional view of the embedded capacitor inside a package under the die shadow

The customized embeddable capacitor has a similar structure to standard MLCC, and is stacked with hi-k dielectric ceramic layers and patterned metal layers alternatively. Unlike simple two terminal ceramic capacitors, however, this embeddable capacitor has through-hole-vias and numerous top and bottom surface electrodes resulting in inherently low inductance (~ 1.5pH). The array capacitor is physically placed in the substrate core, and a polymer molding material is filled between the embedded capacitor and core material. Embedding the ceramic capacitor into the thick server substrate core brings many concerns and issues to overcome such as the coefficient of thermal expansion (CTE) difference of ceramic capacitor, substrate core, molding polymer, and substrate build-up materials, substrate warpage due to embedded capacitors, etc.

Finally, the electrical benefit of a large, low inductance capacitor has been demonstrated. The embedded capacitor dramatically reduces the impedance in the 100 MHz range by the reduction in package inductance. Also, the impedance drop in the 2-10 MHz range has been observed since the embedded capacitor adds to the total amount of package capacitance. The reduction of high frequency impedance results in significant reduction of power supply noise, and this in turn results in improved server product performance.

Embeddable Capacitor Component

Embeddable capacitor component fabrication is based on the combined multi-layer ceramic capacitor (MLCC) and low-temperature-co-firing-ceramic (LTCC) technology. Capacitor fabrication starts with $BaTiO_3$ dielectric powder which is not unique to this customized capacitor, but is a dielectric material of choice in commercial MLCC industry. The pre-milled ceramic powder is mixed with a suitable amount of organics to make a dielectric slip, i.e., green sheet. Nickel paste (internal electrode), is screen printed on this green sheet to form parallel capacitors. The stacked structures of multiple Ni paste and $BaTiO_3$ green sheets are then laminated together and pressed. The number of stack layers and the total layer thickness are pre-determined to achieve a target capacitance value. Similar to LTCC process, the through hole via is formed by laser drilling, and then via is filled with metal. After the surface electrode printing process, the multi-layered green sheet is loaded into a furnace for the firing process.

The fired capacitor is moved to an electro-plating bath for the copper pad formation, and these pads will act as the substrate laser via landing pad. Thus, the dimension, tolerance and thickness of Cu pad are determined by the substrate design rules. After the pad formation, the individual capacitors are separated from each other, and then the manufactured capacitor components are 100% electrically screened for capacitance, dissipation factor and intrinsic resistance values.

The copper pad on the capacitor surface is electrically isolated from the plane surrounding them, and they will be electrically connected to the power rails through the substrate via connection. Furthermore a single capacitor can be internally divided into multiple partitions that are isolated electrically from each other. The partitions are helpful in providing separate capacitances to individual microprocessor cores, multiple power rails, and I/O regions of the die. Theoretically, the array capacitor can be manufactured with many partitions, but the area between the partitions sacrifices the capacitance.

There are several considerations in the design of the surface pads, namely, the laser via landing pad. Laser via diameter drives the pad dimension on the embeddable capacitors to ensure via connectivity and long term reliability. The pad-to-via alignment capability is also a consideration since the laser via is drilled to the capacitor pad and filled with metal. The larger pad dimension would accommodate the required via size easily, however, the pad dimension should be optimized to have the higher capacitance. In addition, the embeddable capacitor placement accuracy, and substrate panel

shrinkage have been considered for the pad designs as shown in Figure 5.

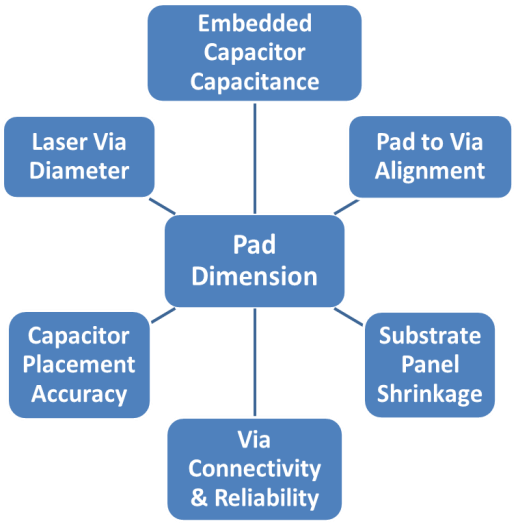

Figure 5. Considerations for the embedded capacitor pad dimension

Package Construction & Assembly

The surface mounting of discrete capacitors is part of the backend process, but the embeddable capacitor is integrated at the initial substrate manufacturing step. At first, the substrate core material is cut to make cavities, and the cavity size is larger than the embeddable capacitor dimension. The capacitor is placed in the substrate cavity, and then a polymer molding material is filled into the cavity between embedded capacitors and substrate core materials. This completes the capacitor embedding process, and the buildup material is then laminated onto the embedded capacitor, and a standard substrate process flow is performed for via connection. The cross sectional view of the completed capacitor embedding into the substrate core and the standard substrate build-up process is shown in Figure 4.

Embedding the large ceramic capacitor into a thick substrate core brings many concerns and issues. First, the coefficient of thermal expansion (CTE) difference of the ceramic capacitor, substrate core, molding polymer, and substrate build-up materials could result in the internal stress and induce the de-lamination at each interface during the standard substrate manufacturing, assembly, and product usage. Therefore, the proper material selection and its interface treatments are essential. Second, embedded capacitors in the substrate core could influence the warpage of substrate, and this could cause first or second level interconnection failures. The number of embedded capacitors and their location should be carefully decided to balance the substrate warpage and the embeddable capacitor performance. Lastly, the rough surface of ceramic capacitors could act as a starting point for cracks to propagate to substrate core or build-up layers. Visual appearance criteria of embedded capacitors are, therefore, more important than surface mounted capacitors.

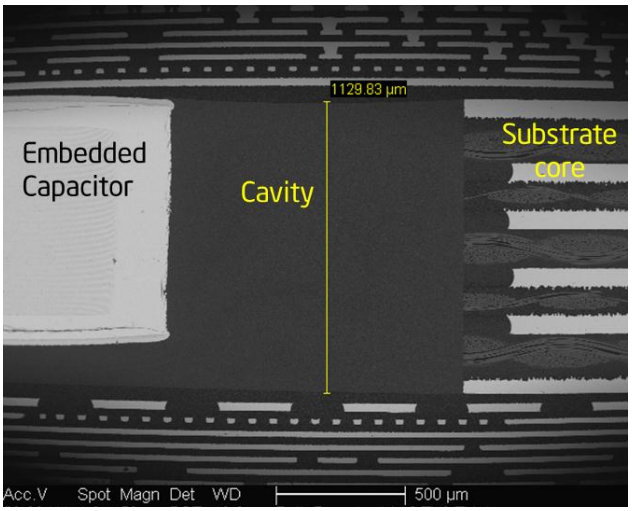

Figure 4. Cross sectional view of embedded capacitor into substrate core

Electrical Performance

To examine the performance of a power delivery network (PDN) design, the Thévenin equivalent impedance looking back into the PDN from the C4 bumps can be measured or simulated [4]. In most cases the PDN design features can be easily resolved and the performance of individual components can be compared. A simplified lumped element model for a typical PDN is shown in Figure 6. Although this model has relatively few components it is typically good enough for purposes of discussion.

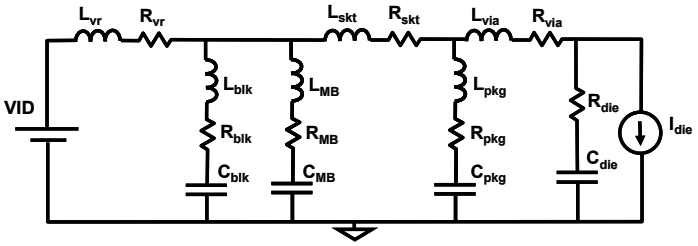

Figure 6. Simplified PDN Model

Historically, the high frequency performance of the power delivery network in packaged microprocessors has not been as good as the low and mid frequency performance. Improvements in voltage regulator (VR) technology, socket technology, package copper thickness, and capacitance density have enabled reductions in the low to mid frequency portion of the power delivery impedance profile. However, the same cannot be said of the high frequency portion of the power delivery impedance profile. The three major factors that determine the high frequency performance are the inductance to the package capacitors, amount of on-die capacitance and the damping provided by the logic's leakage current. While the leakage current has the undesirable effect of cutting into the overall power budget, it does help reduce the first droop peak. Increasing on-die decoupling capacitance (C_{DIE}) is

another way to reduce first droop but there is a die size and leakage penalty associated with it. Reducing the package inductance (L_{PKG}) can be an effective way to address first droop but this is hard to accomplish with traditional decoupling options because the package itself contributes significantly to this inductance, hence improvements gained by reducing the inductance of the individual capacitors is limited. In many cases a significant portion of the die in these advanced microprocessors now sit outside the socket cavity and thus do not have a low inductance path to the package capacitors. The addition of the embedded array capacitor alleviates many of these issues by placing an ultra-low inductance capacitor very close to the die, even when the die overhangs the pin field (Figure 7).

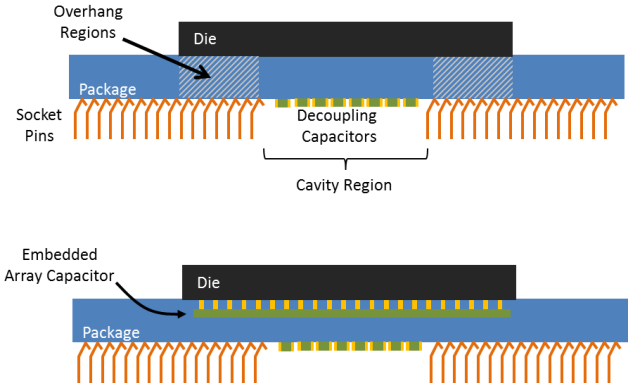

Figure 7. Traditional design with die overhanging cavity region (top), array capacitor embedded in substrate (bottom)

In order to examine the performance provided by the embedded capacitor technology the PDN impedance profile for two test vehicles were measured. The first of these was a traditional microprocessor package with decoupling capacitors in the socket cavity region. The second test vehicle was identical to the first except for the addition of the ceramic array capacitor in the package core. The results of the measurements are shown in Figure 8.

As can be seen from the impedance plot in Figure 8, the embedded array capacitor dramatically reduces the impedance in the 100 MHz range, commonly referred to as *first droop*. It does this by dramatically reducing the inductance between the die and the nearest package capacitance. This reduction in inductance pushes the rising slope of the impedance near 100MHz to the right. Since the die capacitance is constant the right hand side of the first droop peak is mostly unchanged. The end effect is a reduction in the peak height. Similarly, because the array capacitor adds to the total amount of package capacitance, the impedance drop in the 2-10 MHz range (commonly referred to as *second droop*) is pushed to the left, resulting in reduced impedance in this frequency region. Because the voltage seen by the die is the frequency domain current draw multiplied by the impedance profile, reduction of the impedance profile in this way results in reduced voltage noise at the die. Reduced die voltage in turn can be used to either improve the maximum operating frequency of the logic load or it can be used to reduce the nominal DC operating voltage of the logic to reduce overall power consumption. In high premium server application, this first droop reduction by embedded capacitors improves the performance and the server product binning.

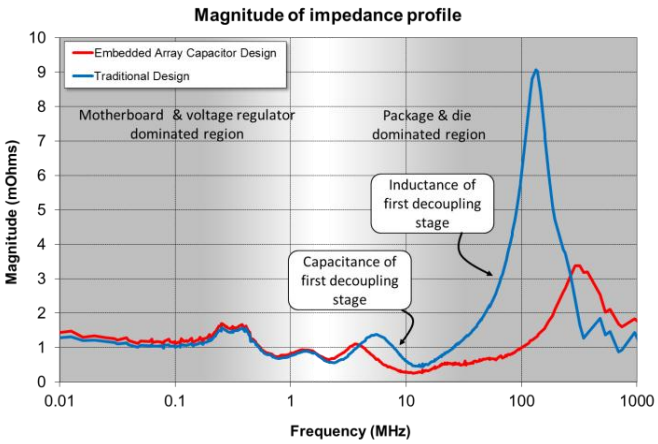

Figure 8. Measured PDN impedances for the embedded array capacitor prototype compared to a traditional design.

Conclusions

We have successfully taken the customized embedded capacitor from the proof of concept stage to an actual product implementation in a high performance server product. The ultra-low inductance embeddable capacitor has been fabricated based on standard MLCC and LTCC technology taking into consideration the compatibility with the microprocessor package structure and manufacturing process. Embedding large ceramic capacitors into thick substrates brings many integration and reliability challenges. The embedded capacitor in substrate core under the die shadow provides low inductance path to the first stage of package decoupling, and adds additional capacitance to the package. This dramatically reduces the high frequency impedance, and ultimately improves the power delivery performance of microprocessors.

Embedded technology has demonstrated performance benefits, but it does increase the package manufacturing cost. Thus, tradeoff studies are necessary for on a given product design to understand if the improved performance and package form factor reduction warrant the additional cost for that specific product or market segment.

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