# Tombstone Initiation Model for Small Form-Factor Surface Mount Passives

Nachiket Raravikar, Rahul Panat, and Susheel Jadhav

***Abstract*— Passive components such as capacitors are shrinking in size in electrical systems in tandem with the device transistor features. With the size shrink comes an increased risk of process-induced defects such as capacitor tombstoning or billboarding. These defects involve poor connectivity of capacitor terminations to the substrates, affecting the electrical performance of the system. We have developed an analytical model to predict the probability of such defects to occur as a function of the design and process factors. The model demonstrates that the surface tension at component terminals dominates over the inertia forces (component weight) in case of components with submilligram weight. Bulkier capacitors have lower risk of tombstoning compared to the lighter ones. The analysis also points to other modulating factors such as component termination width, component height, solder pad size, and the solder paste volume. We also present the experimental results on small form-factor components that confirm some of the predictions for the model. Optimum design guidelines for the electrical systems with soldered components can be obtained from the current model.**

***Index Terms*— Capacitor, Manhattan defect, manufacturing, miniaturization, passives, semiconductor packages, small form factor, solder wetting, tombstone defect, wetting imbalance.**

## I. Introduction

PASSIVES in electrical systems are scaling down as the microprocessors shrink according to Moore's law. A majority of microprocessor passives are surface solder mounted onto the substrate or the motherboard. Other electronic devices such as smartphones, liquid crystal display TVs, and RF controllers also use large numbers of surface mount passives and their miniaturization is ongoing at an unprecedented pace. Since 2006, the environmental regulations have pushed the semiconductor industry toward lead-free solders. Since the number of passives mounted in the electronics industry runs in billions per month, it is very critical to thoroughly understand any failure mechanisms of these components to maintain the electrical performance of the system.

Surface mount passives are designated by a naming system such that a 0402 component indicates a component length of 40 mil and a width of 20 mil. Components such as 0402 and 0603 have a size scale greater than 0.5–1 mm. With miniaturization, the industry is moving to passive form factors (FFs) of 0201 and 01005, where the size scale is of the order of 100–300 $\mu$m. The use of smaller FF passives (capacitors, resistors, and fuses) is expected to increase significantly in the future. Tombstoning (also called Manhattan defect, or in the case of reverse geometry capacitors, the billboarding defect) is one of the major defects that involves lifting of one of the ends of the passives during solder attach. The driving force for tombstoning is the differential wetting of the component when it passes through the reflow oven [1]–[4]. In the past, the source of this differential wetting was believed to be the differential temperature of the two solders as the component passes through the reflow oven. Fig. 1 shows the case of tombstoning of a small 0201 capacitor after lead-free solder reflow. One end of the capacitor is seen lifted with the other end acting as a pivot. This defect will give rise to yield losses and/or touch-up, affecting the throughput time and increasing cost, besides affecting the electrical performance if undetected.

Fig. 2 shows passive components in two different orientations going through the reflow oven. The passive parallel to the reflow direction is expected to have its terminal solder in the reflow direction melted first. The resulting surface tension moment drives the opposite end of the passive to lift, that is, to tombstone. For the passive perpendicular to the reflow direction, the probability of tombstoning is lower with the solder at both the terminals melting at about the same time. The obvious consequence of this mechanism has been that the passives mounted perpendicular to the movement of the board in the reflow oven show less tombstoning when compared to the passives mounted parallel to the reflow direction [2]. This was certainly true when the passives were large in size—0603 and larger. Accordingly, the models to predict tombstone initiation assumed wetting only on one terminal [2]–[4]. New experimental evidence suggests that the direction dependence of the tombstoning defect is no longer valid for smaller passives such as 01005 or 0201 [5]. Obviously, the assumption that one end of the passive melts completely, while the other end does not, may not entirely be true for these passives. Experimental evidence points to one end of the passive completely wetting, while the other end only does so in a partial manner. Fig. 3 shows wetting on both terminals for a tombstoned 0201 capacitor. Remnants of the meniscus formed before lifting can be seen on the left. Another important observation is that in the small components, the solder beneath the termination is insignificant at tombstone initiation time (when the component is horizontal) and plays a role in tombstone dynamics, but not so much in tombstone initiation.

Shrinking of the passive size has also given rise to other issues in the assembly process not seen in large capacitors.

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Fig. 1. Optical image and cross-section of a 0201 capacitor lifted after solder reflow [1].

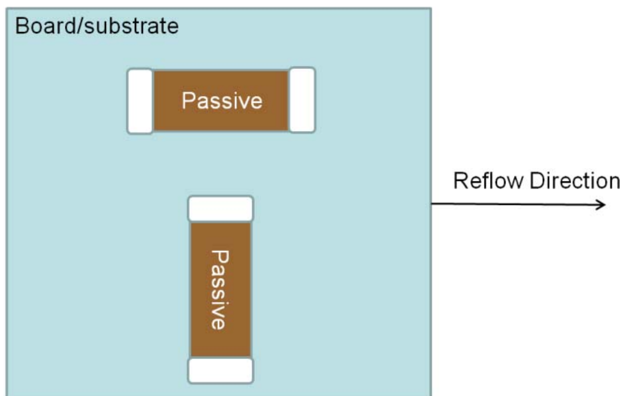


Fig. 2. Schematic showing the orientation of the passive as it passes through the reflow oven.

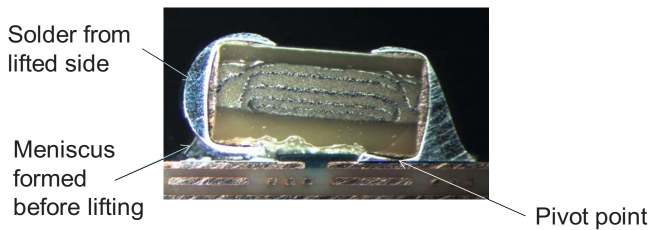


Fig. 3. Wetting on both terminals of a 0201 capacitor tombstoned during solder reflow [1]. Remnants of the meniscus formed before lifting can be seen on the left. An extrapolation from this meniscus indicates around 20%–25% wetting on the lifting side before tombstoning.

For example, any defects or disturbances in the lead-free metallization of capacitor terminals (typically a low-melting-point metal, such as Sn [6], [7]) can become significant if the terminals shrink with the capacitor FF [8]. Such disturbances are not an issue for large FF capacitors due to their relative size compared to the overall termination. With the smaller terminal size, these disturbances or defects can inhibit the wetting of the solder with the terminal. Further, if the defects are asymmetric, they can give rise to differential wetting resulting in increased propensity for tombstoning.

Another difference in smaller and larger passives is the relative size of the termination width with respect to the terminal dimension. This factor was neglected in the prior models assuming the factor to be negligible. Table I shows the nominal capacitor width to terminal width ratio ($W/T_w$) for various capacitor FFs. Clearly, the fraction of $T_w$ versus $W$

TABLE I
LIST OF COMMON CAPACITOR TYPES USED IN THE INDUSTRY WITH CAPACITOR WIDTH AND TERMINATION WIDTH VALUES

| Capacitor type | Termination width (nominal) $T_w$ (mm) | Capacitor width (nominal) $W$ (mm) | $W/T_w$ |
|---|---|---|---|
| 01005 | 0.1 | 0.2 | 2 |
| 0201 | 0.15 | 0.3 | 2 |
| 0402 | 0.25 | 0.5 | 2 |
| 0603 | 0.25 | 0.8 | 3.2 |
| 0805 | 0.25 | 1.25 | 5 |
| 1210 | 0.5 | 2.5 | 5 |

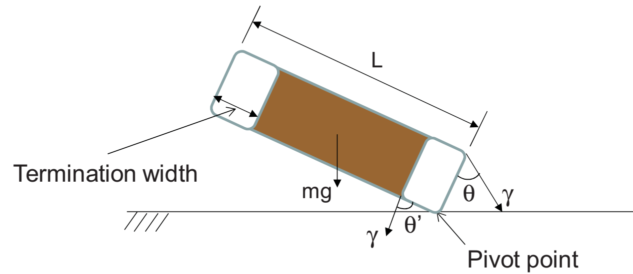


Fig. 4. Schematic of the tombstoning model suggested by Wassink and Verguld [3].

is significant for 0402 and smaller capacitors. If wetting occurs on both the ends of the capacitor, we have to account for the termination width, which is expected to play a significant role as shown in the model and experimental data later in this paper.

Lastly, we postulate that the small FF passives will be vulnerable to any imbalance in wetting caused by various triggers due to their low weight. For example, any difference in the wetting speed of the solder at two passive terminals will give rise to different contact angles resulting in tombstoning, simply due to the very low weight of the small FF caps. To give some idea, the mass of a 0201 capacitor (0.32 mg) [9] is around 30× less than that for a 0603 capacitor (10 mg) [10].

## II. PAST THEORY AND EXPERIMENTS

Wassink and Verguld [3] presented their tombstoning model where they calculated the tombstoning propensity by assuming wetting only on one side of the capacitor. The moment to lift the capacitor was assumed to be driven by the solder surface tension. Fig. 4 shows a schematic of such a situation, where $\gamma$ is the surface tension of the solder. A simple moment balance can give the propensity for tombstoning. The forces they considered were the solder surface tension and the capacitor weight.

Wassink and Verguld [3] compared the propensity for tombstoning on 1206 and 0805 resistors for different angles of wetting. Hui and Ralph [2] used the simple model by Wassink and Verguld [2] and plotted the relative tendency for tombstoning. They also carried out experiments for large passives and different pad geometries. They used 1206 and 1210 resistors; 0805, 1206, and 1812 capacitors; and 3216, 6032, and 7243 components. They observed that the lifting moment increases with the contact angle, which in turn

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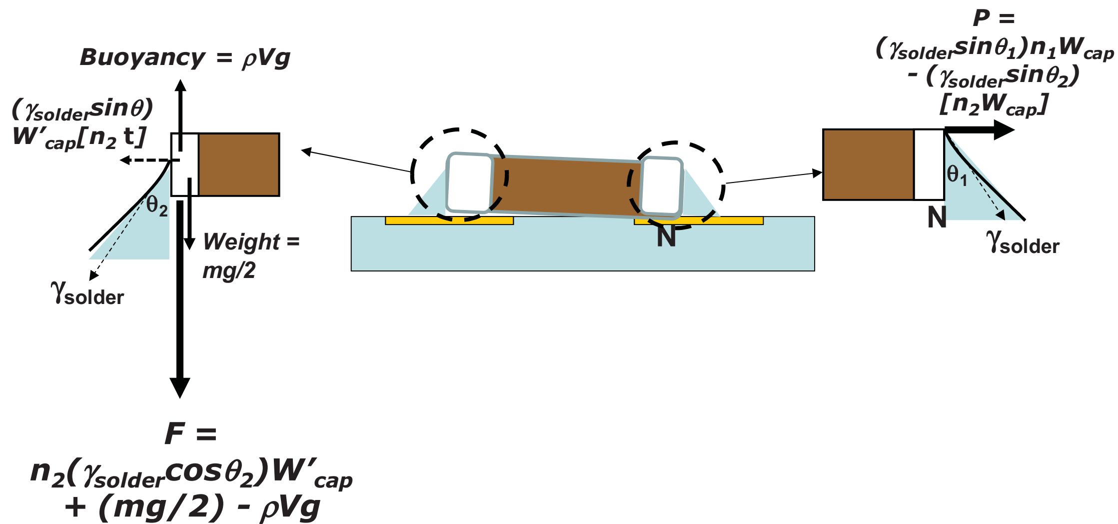


Fig. 5. Schematic of the tombstoning initiation model.

increases with the printed circuit board land length protruding from the end of the component.

Experimental work on surface mounting of smaller caps, namely, 0201 caps and 01005 caps, was done recently [1], [9], [11], [12]. Ramkumar *et al.* [9] evaluated the tombstoning performance of 0201 caps for four pad designs, two pad layouts, five pad surface finishes, three solder alloys, and two different soldering stencil thicknesses. This extensive experiment showed that for all the cases, the defect rate was not correlated with the orientation of the capacitor going into the oven (see Fig. 1). Neathway *et al.* [12] found that the tombstoning of 0201s was affected by the orientation of the capacitor when it enters the reflow oven. However, their data was confounded with the placement offset—no tombstoning was observed when the placement offset was removed.

## III. Model and Experiments

We assume a small passive with one end completely wet with solder as shown in Fig. 5. The other end of the passive is only partially wet. The forces to lift the passive, as shown in Fig. 5, are the solder surface tension on the side with point N as shown in Fig. 5, and the buoyancy force at the other end of the capacitor. The passive weight and the solder wetting at the tipping side will prevent tombstoning.

We consider only the initiation point for tombstoning. Also, we consider a near horizontal passive with very little solder underneath, consistent with observations on small passives [1], [5]. To induce asymmetry in the model, we take the fraction of the wetted thickness of the passive at the tipping side as less than that at the side with point N.

At tombstone initiation, the tipping point N is at the corner with full solder wetting. All the moments are measured about this point. At the instant of tipping, the net lifting moment $\tau_N$ is

$$\tau_N = (n_1 \sin\theta_1 - n_2 \sin\theta_2)\gamma_{\text{solder}} W_{\text{cap}} t - (n_2 \cos\theta_2)\gamma_{\text{solder}}[W_{\text{cap}} + 2T_w]L - \frac{mgL}{2} + \rho V g L \quad (1)$$

where

- $\gamma_{\text{solder}}$ surface energy of the solder material in N/m;
- $n_1$ fraction of solder height at the terminal with pivot point (taken as 1, i.e., full wetting based upon experimental data to date);
- $n_2$ fraction of the solder height on the tipping side;
- $m$ mass of the passive in kilograms;
- $\rho$ density of the solder in kg/m$^3$;
- $V$ volume of the solder displaced by the passive in cubic meters;
- $T_w$ termination width of the passive in meters (see Fig. 4);
- $L$ length of the passive in meters;
- $t$ thickness of the passive in meters;
- $W_{\text{cap}}$ width of the passive in meters (in the plane of this paper in Fig. 5);
- $\theta_1, \theta_2$ contact angles of the solder as shown in Fig. 5.

If $\tau_N$ is positive, tombstoning will occur and vice versa. Note that the solder wets along the termination on both side of the passive. However, only the wetting from the lifting side will contribute to the moment about point N, preventing the passive tombstoning. The moment due to wetting on the passive termination width will contribute to the twisting of the passive (also observed as one of the defects) but not so much to the tombstoning phenomenon. Note that for small FF passives, the angles $\theta_1$ and $\theta_2$ will be higher than that for large FF passives. This is because of the larger thickness of the large FF passives.

This simple model takes into account the effects of the substrate pad and solder volume in an indirect manner. It was shown in experiments [1] that longer the pad extends beyond the passive termination, higher is the driving force for tombstoning. Obviously, wider substrate pad (longer along the passive axis) or a higher wetting speed on the pad or higher solder volume will increase the angles $\theta_1$ and $\theta_2$. For any asymmetry in wetting, this will result in an increased driving force for tombstoning. The fraction $n_2$ takes into account the partial wetting of the solder along the passive thickness $t$ as

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TABLE II
MASS IN MILLIGRAMS FOR VARIOUS FF PASSIVES [9], [13]–[15]

| Capacitor FF | Mass (mg) |
|---|---|
| 01005 | 0.004 |
| 0201 | 0.32 |
| 0402 | 1.6 |
| 0603 | 3.2 |
| 0805 | 47 and 22 |

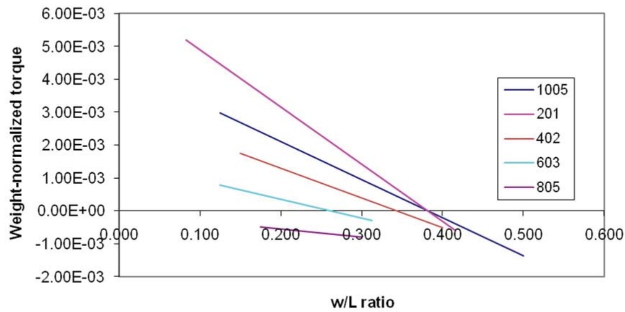


Fig. 6. Shorter termination widths and/or longer capacitors have a high risk of tombstoning. Bulkier capacitors buy more tombstoning margin over lighter ones.

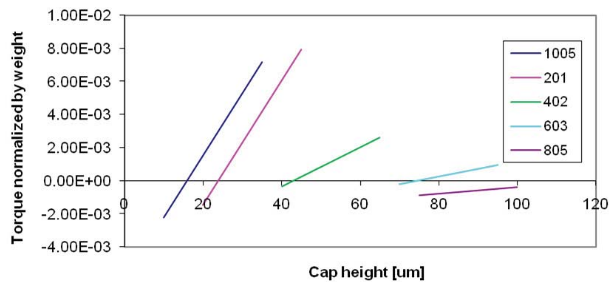


Fig. 7. Bulky capacitors buy more tombstoning margin over lighter capacitors.

well as any defects in the termination [8]. Note that the model takes into account the surface tension forces of the solder when it is molten and not creep effects that occur over long periods of time after the solder has been solidified.

The $\gamma_{\text{solder}}$ at around 200 °C–250 °C varies from 0.46 N/m for pure Pb to 0.567 N/m for pure Sn [16], [17]. For lead-free solders such as SnCu and SnAg, the value is at the higher end of this range [18] at around 0.52–0.55 N/m. The contact angles can vary with the solder volume, termination size, pad location and size, and the properties of the solder and the pad [2], [4]. Generally, the contact angle can have a wide range from 15° to 60°. The fraction $n_1$ is taken as unity—assuming full wetting on the side of the pivot point N. The fraction $n_2$ will be examined from zero to unity. The $n_2$ of zero indicates no wetting on the lifting side, while $n_2$ of 100% indicates equal wetting on both sides so no tombstoning can occur. Mass $m$ of the passive depends upon the FF. Table II shows the mass of different capacitors from 01005 to 1210 FFs.

We carried out experiments to confirm the modeling predictions for tombstoning trends. A next-generation Intel microprocessor with 0201 capacitors from different suppliers

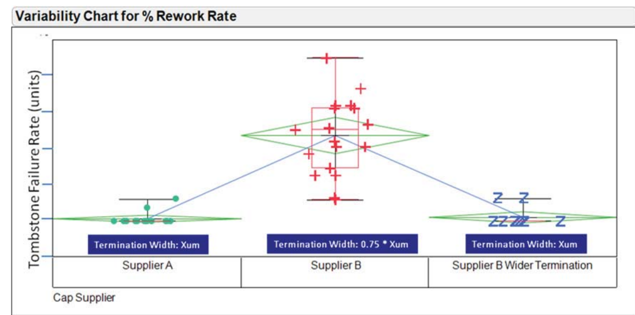


Fig. 8. High tombstoning failure rate is seen for 0201 capacitor when the termination width is decreased by 25% with all other parameters remaining constant. The data confirms the trends predicted by the model (see Fig. 6).

was used. Different pad sizes were evaluated. The factors we varied included the capacitor termination width, amount of solder volume, pad size and shape, and gold thickness on the base motherboard. We will present the general trends of our findings in Section IV.

The length, width, thickness, and termination width of the various FF capacitors are taken from passive manufacturer data sheets [19].

## IV. MODELING RESULTS AND COMPARISON WITH EXPERIMENTS

The results of our modeling are shown in the plots in Figs. 6, 7, and 9(a) and (b). These plots predict the risk or propensity toward tombstoning of any capacitors as a function of design and process factors. In general, a positive tombstone torque indicates a finite tombstone risk. The data points showing negative tombstone torque show no tombstone risk. The tombstone torque is weight averaged, so that all capacitor FFs can be compared together.

Fig. 6 indicates that tombstoning risk increases as the terminal width to capacitor length ($T_w/L$) ratio decreases. This shows that for a given capacitor length, shorter terminal widths will increase the tombstone risk. According to the modeling results in Fig. 7, everything else being the same, the tombstone risk increases for taller capacitors than for shorter capacitors. Fig. 8 indicates that larger pads tend to increase the tombstone risk, in general. However, according to Fig. 8(b), if the solder coverage on the higher wetting side decreases from 100% to 50%, then tombstone risk decreases. Such coverage decrease could be a result of lower paste volume. This indicates that tombstone risk can be decreased for larger pads by using lower paste volumes. For all cases, the lighter capacitors such as 0201 and 01005 are more sensitive to the above design and process changes.

Fig. 8 shows that by reducing $T_w$ by 25%, the tombstone failure rate is significantly increased when all other variables are kept constant. This is in line with the predictions made in Fig. 6. Another observation is that the spread in tombstoning defect rate has also increased with a reduction in $T_w$. These results also correlate with experimental evidences presented in the literature [1]–[7].

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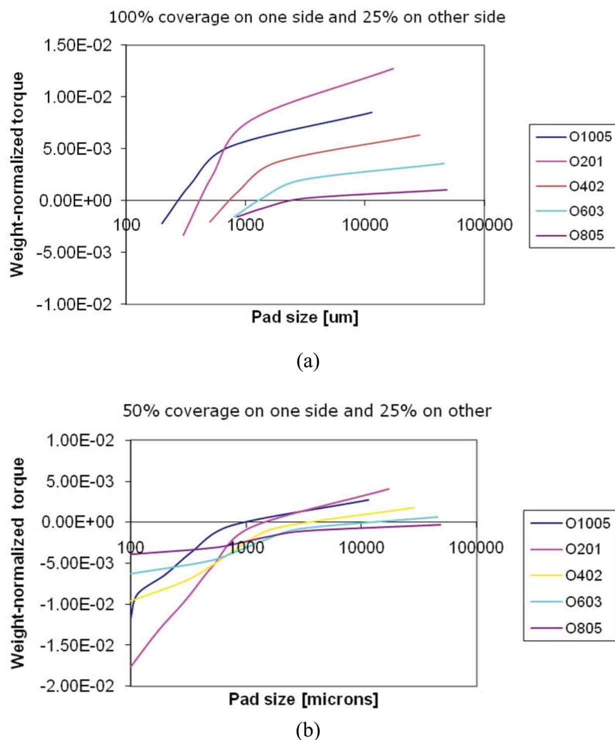


Fig. 9. Tombstoning risk as a function of pad size for different passive form-factors. Tombstoning risk increases with pad size, especially along the length of the capacitors. Bulkier capacitors buy more tombstoning margin over lighter ones. Also, tombstoning risk decreases as the relative difference in the wetting of the two capacitor terminals decreases from 75% to 25%.

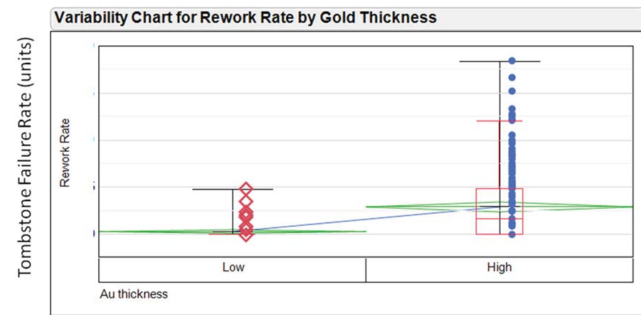


Fig. 10. Tombstoning rate comparison between low and high gold thickness of the base motherboard with all other variables being kept constant.

The mechanism of tombstoning is fundamentally the imbalance of forces on either sides of the capacitor resulting in a torque that is sufficient to lift, move, or topple the capacitor. The shorter terminal widths would further exacerbate imbalance because they allow relatively insufficient solder coverage. Longer capacitors offer longer moment arm for the torque, and thus a relatively lower load $F$ in (1) may be sufficient to prevent tombstoning. Similarly, taller capacitors offer longer moment arm $t$ for force $P$ in (1). Thus, tombstoning may occur at a relatively lower $P$ for taller capacitors

With existing difference in solder wetting, the larger solder angles at the capacitor terminals would generally increase the tombstone risk further. Such a scenario may exist for the case with large pads and large enough paste volumes such that around 75% difference in solder coverage between two terminals of capacitors would cause tombstoning. The way to overcome the tombstone risk due to large pad sizes is to reduce paste volume, so that the probability of 75% solder coverage difference between two terminals would decrease. As shown in Fig. 9, the tombstone risk for large pads can be reduced if the solder coverage at two terminals is comparable. It is interesting to note that complete solder coverage of terminals is not required to reduce tombstone risk. What is important is equivalent solder coverage on both capacitor terminals.

Fig. 10 shows the tombstoning rate comparison between low and high gold thickness of the base motherboard with all other variables being kept constant. The high gold thickness can cause faster wetting of the solder and hence greater possibility of $(\theta_1 - \theta_2)$ making the system more unstable, especially for small FF components. Clearly, the tombstoning rate is higher for thicker gold than thinner gold thickness of the board. Note that the ratio of Au thickness between thicker and thinner boards is around 5 in Fig. 10.

Fig. 10 shows the tombstone rate for different paste volumes (thick versus thin stencil thickness) and pad dimensions. The model from (1) does not directly talk about the effects of solder paste volume and board pad dimensions. However, a faster spread of solder over the pad would increase $\theta_1$ and $\theta_2$ at a faster rate than usual and cause the system to be more unstable. At the same time, larger solder volume can also have the same effect. On the other hand, larger solder volume may also provide a greater stability (from solder tackiness) to the terminal. These competing factors make exact predictions difficult to make. Clearly, further work is needed in this regard that takes into account the wetting speed of the solder paste and the *in situ* $\theta_1 - \theta_2$ to predict the tombstoning defect rate.

Lastly, all the plots show that tombstoning initiates late for bulkier capacitors such as 0603 and 0805 than for lighter capacitors such as 0201 and 01005. For lighter capacitors the weight term (milligram) is so small that it is almost negligible relative to other interface interaction terms in (1). For bulkier capacitors, the weight term is not always negligible. This indicates that, all other factors being the same, tombstone margin can be improved by increasing the capacitor weight.

## V. Conclusion

As future package passive components continue to scale down, capacitor tombstone defect risk will increase because weight alone cannot prevent it. Bulkier capacitors gain a lot more tombstone margin, relative to lighter capacitors. We developed an analytical model, based on which, it is clear that tombstone risk for lighter capacitors can be minimized by increasing their terminal width, decreasing height, using relatively lower paste volume, and ensuring equivalent wetting on either sides of the capacitor terminals.

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