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(54) Title: NANOWIRES COATED ON TRACES IN ELECTRONIC DEVICES

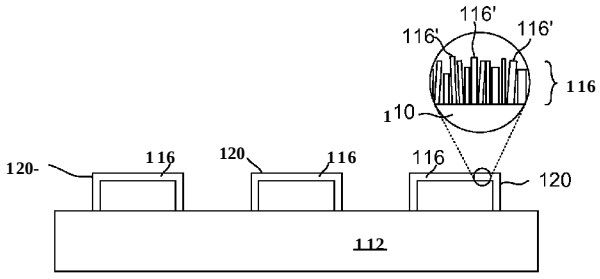


Fig. 3C

(57) Abstract: Methods and devices including the formation of a layer of nanowires on wiring line traces are described. One device comprises a first dielectric layer and a plurality of traces on the first dielectric layer, the traces comprising Cu. The traces include a layer of ZnO nanowires positioned thereon. **A** second dielectric layer is positioned on the first dielectric layer and on the traces, wherein the second dielectric layer is in direct contact with the ZnO nanowires. Other embodiments are described and claimed.

NANOWIRES COATED ON TRACES IN ELECTRONIC DEVICES

BACKGROUND

Signals in electronic devices may be carried by wiring line traces made of materials such as copper (Cu). As electronic devices are typically multilayered in structure, the traces may be sandwiched between dielectric layers. As the size and spacing between traces shrinks and the electrical signaling speed increases with each technology generation, problems due to interactions between adjacent traces, or interactions between the trace and the overlying dielectric layer, may lead to electrical and/or mechanical problems.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments are described by way of example, with reference to the accompanying drawings, which are not drawn to scale.

Figure 1A illustrates a view of ZnO nanowires formed on a fiber.

Figure IB illustrates a more magnified view of the nanowires of Figure 1A.

Figure 2 illustrates a view of a nanowire coated trace on a dielectric layer, in accordance with certain embodiments.

Figure 3A illustrates a cross-sectional view of a substrate having a plurality of traces thereon, in accordance with certain embodiments.

Figure 3B illustrates a cross-sectional view of the traces of Figure 2A being placed into a chemical bath, in accordance with certain embodiments.

Figure 3C illustrates a cross-sectional view of the traces of Figure 2B with a nanowire coating formed thereon, in accordance with certain embodiments.

Figure 3D illustrates a cross-sectional view of the nanowire coated traces of Figure 2C with a dielectric layer deposited thereon, in accordance with certain embodiments.

Figure 4 illustrates a flowchart of operations for forming structures including nanowire coated traces, in accordance with certain embodiments.

Figure 5 illustrates an electronic system arrangement in which embodiments may find application.

DETAILED DESCRIPTION

Reference below will be made to the drawings wherein like structures may be provided with like reference designations. In order to show the structures of various embodiments most clearly, the drawings included herein include diagrammatic representations of electronic device

and integrated circuit structures. Thus, the actual appearance of the fabricated structures may appear different while still incorporating the claimed structures of the illustrated embodiments. Moreover, the drawings may show only the structures necessary to understand the illustrated embodiments. Additional structures known in the art have not been included to maintain the clarity of the drawings.

Certain embodiments relate to the formation of wiring line traces that offer improved electrical and mechanical properties. Such embodiments include the formation of nanowires on the traces. Certain embodiments as described herein include the formation of zinc oxide (ZnO) nanowires on traces formed from materials such as copper. The zinc oxide nanowire coated wiring traces display desirable electrical and mechanical properties. For instance, zinc oxide may act as a diffusion barrier for copper. In addition, the nanowires provide good adhesion between the trace and the overlying dielectric material.

Figure 1A illustrates a photomicrograph of a layer of ZnO nanowires grown on a carbon fiber. Figure 1B illustrates a more magnified view of the zinc oxide nanowires of Figure 1A. The ZnO nanowires have a structure that includes a relatively large surface area.

As traces become closer and closer together, problems such as metal diffusion from one trace to another may arise. The diffusion of metal from one trace to another can lead to problems with shorting between the traces. By coating the wiring traces with ZnO nanowires, the diffusion of copper between traces may be inhibited, thus decreasing the risk of electrical shorting. This enables the traces to be formed closer together than would otherwise be possible.

During high speed signal transmission, the surface condition of the trace may be relevant to its ability to efficiently transmit current and limit signaling insertion loss. As the electrical input/output signaling gets faster, current tends to be concentrated at or near the skin (outer metal surface) of the trace due to skin effect. In general, it is observed that the smoother the skin, the less the signal insertion loss at high frequencies. However, if the skin is too smooth, there may be poor adhesion between the trace and the overlying dielectric layer. Poor adhesion may lead to voids/delamination and the like being formed in the structure, which can lead to both mechanical and electrical problems. Coating the trace with nanowires can enable the presence of a relatively smooth skin of metal for limiting signal insertion loss, while at the same time the nanowires provide enhanced mechanical coupling to the overlying dielectric layer. The rod-like structure of the plurality of nanowires acts to mechanically interlock the trace to the dielectric layer. This mechanical interlocking inhibits pull-away of the dielectric layer from the traces, thus improving the mechanical properties and reliability of the structure while enabling smoother traces for higher speed signal transmission.

Figure 2 illustrates a view of a nanowire coated trace 20 on a substrate 12, in accordance with certain embodiments. The nanowire coated trace 20 may comprise a metal such as Cu having a layer of nanowires 16' extending outward from one or more surfaces thereof. As illustrated in Figure 2 in the blown up portion, the nanowire coated trace 20 includes individual nanowires 16' that are formed on the surface of the metal of the trace. In the embodiment illustrated in Figure 2, the nanowire coated trace 20 includes a plurality of surfaces having the nanowires 16' extending outward therefrom.

Figures 3A - 3D illustrate certain operations including the formation of nanowires on traces and a dielectric layer on the nanowire coated traces, in accordance with certain embodiments. Fig. 3A illustrates wiring traces 110 on a dielectric layer 112. The traces 110 may be formed from any suitable electrically conductive material, for example, a metal such as Cu. The term metal as used herein includes pure metals and alloys. The traces 110 may make electrical contact with layers below (and after subsequent processing of layers above) in order to transmit electrical signals through the device.

The dielectric layer 112 may be formed from any suitable insulating material, for example, a build-up layer such as Ajinomoto Build-up Film (ABF), available from Ajinomoto Fine-Techno Co., Inc. In certain embodiments, the dielectric material may be an epoxy with fillers. The traces may have a variety of geometries, including, but not limited to, a rectangular cross section as illustrated in Figure 3A.

A nanowire layer 116 may be formed on the traces 110. The nanowire layer may be formed using any suitable method. In one suitable method, as illustrated in Figure 3B, the traces 110 on the dielectric layer 112 may be dipped in a solution 114 in a bath-based process. The solution 114 may include zinc nitrate hydrate and hexamethylenetetramme (HMTA) and be kept at a temperature of about 90°C. Such conditions result in the growth of nanowire layer 116 on the traces 110, to form nanowire coated traces 120 as illustrated in Figure 3C. The areas of the dielectric 112 not covered with traces 110 may be shielded from solution using a photolithographic film so that it does not get coated with the nanowires. This can be done using suitable photolithographic methods. In other embodiments, the nanowires may be coated on the exposed dielectric layer 112, with no added benefit or harm to the subsequent dielectric layer formations or to the functioning of the semiconductor package. As illustrated in the blown-up portion of Figure 3C, the nanowire layer 116 includes a plurality of individual nanowires 116'. Using the chemicals above, the nanowire coated traces 120 will comprise individual ZnO nanowires 116'formed on the Cu traces 110, as illustrated in the blown up portion of Figure 3C. In certain embodiments, the entire substrate 112 with traces may be immersed in the chemical

bath to form the nanowire layer on the traces 110. Areas on the substrate not to be coated with the nanowires may be covered using suitable lithographic methods.

The nanowires 116' may be sub-micron in size, with certain embodiments including a range of 100-1000 nm (nanometers) in length and 10-50 nm in diameter. Other sizes are also possible. The nanowires generally grow in a substantially perpendicular direction to the surface, as illustrated in Figure 3C, though certain embodiments may have a different growth pattern. As illustrated in Figure 3D, the next dielectric layer 122 may then be formed on the nanowire coated traces 120. The dielectric layer 122 may be formed from any suitable insulating material, including, but not limited to, polymers, for example, ABF, which is an organic resin with fillers.

A flowchart of operations in accordance with certain embodiments is set forth in Figure 4. Box 200 is supplying a substrate. The substrate may be in the form of a panel of substrates. In certain embodiments the substrate comprises a dielectric layer such as a polymer with fillers. Box 202 is forming wiring line traces on the substrate. The traces may be formed on a dielectric layer and may be formed using any suitable procedure, including, but not limited to, deposition of a metal layer followed by masking and etching. Box 204 is forming nanowires on the wiring line traces, using a wet bath process such as described above or using any other suitable process for forming nanowires. The nanowires may be formed to have a morphology that is substantially rod-like in shape, through other shapes may also be possible. Box 206 is depositing a dielectric layer on the nanowire coated wiring line traces. Such a dielectric layer may be deposited so that there is a mechanical interlocking with the nanowires. This leads to a good bond between the dielectric layer and the traces. The dielectric layer may be formed from any suitable material, including, but not limited to polymers with fillers. Examples may include build-up materials such as ABF or a photoresist. Box 208 is forming additional wiring line traces on the dielectric layer that is on the coated wiring line traces, if desired, and then forming nanowires on the additional wiring line traces as in Box 204. Multiple layers of coated wiring lines may be formed with multiple dielectric layers. In certain embodiments, such layers may be laminated to form a multilayer structure.

It should be noted that the terms "trace", "traces", "wiring", "line" and combinations of these terms relate to the electrically conductive path extending in an electronic device. In certain embodiments, any metal structure where fine spacing is necessary may benefit from having the nanowire layer formed thereon.

The nanowires coated on the traces may in certain embodiments be formed from ZnO, but are not limited to ZnO. Other materials are also possible, as a variety of materials can be grown as nanowires in accordance with suitable procedures. ZnO has advantages, as noted above, of

both forming the nanowire structure that enhances the mechanical connection between the dielectric and the trace, as well as acting as a diffusion barrier for the trace metal. In addition, a variety of electrically conducting materials may be used as trace materials in addition to Cu. One example of a metal that may be used as a trace material is silver (Ag).

Embodiments including coated wiring traces may include traces on a variety of substrates, including, but not limited to, package substrates, semiconductor substrates, and printed circuit board substrates. Moreover, coated traces may be used at a variety of levels within the devices, including those within a stack of layers and those on or near the outermost surface(s) of a body.

Embodiments including coated wiring traces may be used in a variety of structures have a variety of line widths and trace widths. For example, certain embodiments may be used for line spacings and line widths in the range of 1 to 10 μιη (microns). Other line spacings and line widths, larger and smaller, are also possible.

Assemblies including structures formed as described in embodiments above may find application in a variety of electronic components. Figure 5 schematically illustrates one example of an electronic system environment in which aspects of described embodiments may be embodied. Other embodiments need not include all of the features specified in Figure 5, and may include alternative features not specified in Figure 5.

The system 301 of Figure 5 may include at least one central processing unit (CPU) 303. The CPU 303, also referred to as a microprocessor, may be a die attached to a package substrate 305, which is then coupled to a printed circuit board 307 (for example, a motherboard). The CPU 303, as well as the package substrate 305 and the printed circuit board 307, are examples of assemblies that may be formed in accordance with embodiments such as described above, to include wiring line traces including a nanowire layer. A variety of other system components, including, but not limited to memory and other components discussed below, may also include structures formed in accordance with embodiments such as described above.

The system 301 may further include memory 309 and one or more controllers 311a, 311b … 31In, which are also disposed on the motherboard 307. The motherboard 307 may be a single layer or multi-layered board which has a plurality of conductive lines that provide communication between the circuits in the package 305 and other components mounted to the board 307. Alternatively, one or more of the CPU 303, memory 309 and controllers 311a, 311b … 31In may be disposed on other cards such as daughter cards or expansion cards. The CPU 303, memory 309 and controllers 311a, 311b … 311n may each be seated in sockets or may be connected directly to a printed circuit board or all integrated in the same package. A display 315 may also be included.

Any suitable operating system and various applications execute on the CPU 303 and reside in the memory 309. The content residing in memory 309 may be cached in accordance with known caching techniques. Programs and data in memory 309 may be swapped into storage 313 as part of memory management operations. The system 301 may comprise any suitable computing device, including, but not limited to, a mainframe, server, personal computer, workstation, laptop, handheld computer, netbook, tablet, book reader, handheld gaming device, handheld entertainment device (for example, MP3 (moving picture experts group layer - 3 audio) player), PDA (personal digital assistant) telephony device (wireless or wired), network appliance, virtualization device, storage controller, network controller, router, etc.

The controllers 311a, 311b … 311n may include one or more of a system controller, peripheral controller, memory controller, hub controller, I/O (input/output) bus controller, video controller, network controller, storage controller, communications controller, etc. For example, a storage controller can control the reading of data from and the writing of data to the storage 313 in accordance with a storage protocol layer. The storage protocol of the layer may be any of a number of known storage protocols. Data being written to or read from the storage 313 may be cached in accordance with known caching techniques. A network controller can include one or more protocol layers to send and receive network packets to and from remote devices over a network 317. The network 317 may comprise a Local Area Network (LAN), the Internet, a Wide Area Network (WAN), Storage Area Network (SAN), etc. Embodiments may be configured to transmit and receive data over a wireless network or connection. In certain embodiments, the network controller and various protocol layers may employ the Ethernet protocol over unshielded twisted pair cable, token ring protocol, Fibre Channel protocol, etc., or any other suitable network communication protocol.

Terms such as "first", "second", and the like may be used herein and do not necessarily denote any particular order, quantity, or importance, but are used to distinguish one element from another. Terms such as "top", bottom", "upper", "lower", "overlying", and the like may be used for descriptive purposes only and are not to be construed as limiting. Embodiments may be manufactured, used, and contained in a variety of positions and orientations.

In the foregoing Detailed Description, various features are grouped together for the purpose of streamlining the disclosure. This method of disclosure is not to be interpreted as reflecting an intention that the claimed embodiments of the invention require more features than are expressly recited in each claim. Rather, as the following claims reflect, inventive subject matter may lie in less than all features of a single disclosed embodiment. Thus the following

claims are hereby incorporated into the Detailed Description, with each claim standing on its own as a separate preferred embodiment.

While certain exemplary embodiments have been described above and shown in the accompanying drawings, it is to be understood that such embodiments are merely illustrative and not restrictive, and that embodiments are not restricted to the specific constructions and arrangements shown and described since modifications may occur to those having ordinary skill in the art.

What is claimed:

1. A device comprising:

a substrate;

a trace comprising a metal positioned on the substrate; and

a layer of nanowires positioned on the metal trace.

2. The device of claim 1, wherein the nanowires are in direct contact with the trace.

3. The device of claim 1, wherein the substrate comprises a first dielectric layer, the device further comprising a second dielectric layer positioned on the nanowires and on the first dielectric layer.

4. The device of claim 3, wherein the trace includes a first surface in direct contact with the first dielectric layer, and wherein the second dielectric layer is in direct contact with the nanowires.

5. The device of claim 3, wherein the trace includes a plurality of additional surfaces that are not in direct contact with the first dielectric layer, and wherein the nanowires are positioned in direct contact with the additional surfaces.

6. The device of claim 1, wherein the nanowires comprise zinc oxide.

7. The device of claim 1, wherein the trace comprises Cu.

8. The device of claim 1, wherein the substrate comprises a dielectric material.

9. The device of claim 1, wherein the substrate comprises a semiconductor material.

10. The device of claim 1, wherein the substrate comprises a semiconductor material, the device further comprising a dielectric layer on the semiconductor material, and wherein the trace is positioned on the dielectric layer.

11. The device of claim 1, wherein the trace includes a plurality of surfaces on which the nanowires are positioned.

12. A device comprising:

a first dielectric layer;

a plurality of traces on the first dielectric layer, the traces comprising Cu;

the traces including a layer of ZnO nanowires thereon; and

a second dielectric layer positioned on the first dielectric layer and on the traces, wherein the second dielectric layer is in direct contact with the ZnO nanowires.

13. The device of claim 12, wherein the device comprises a package substrate.

14. The device of claim 13, wherein the first dielectric layer and the second dielectric layer comprise an organic polymer material with fillers.

15. The device of claim 12, wherein the nanowires have a length of no greater than 1 μιη.

16. A method for forming an electronic device, comprising:

providing a first dielectric layer;

providing a metal trace on the first dielectric layer;

providing a layer of nanowires on the metal trace on a substrate; and

positioning a second dielectric layer on the first dielectric layer and on the metal trace, wherein the second dielectric layer covers the nanowires on the metal trace.

17. The method of claim 16, further comprising:

providing an additional metal trace on the second dielectric layer;

providing a layer of nanowires on the additional metal trace; and

providing a third dielectric layer on the second dielectric layer and on the additional metal trace, wherein the third dielectric layer covers the nanowires on the additional metal trace.

18. The method of claim 10, wherein the nanowires comprise zinc oxide and the metal trace comprises Cu.

19. The method of claim 10, wherein the electronic device comprises a semiconductor.

20. The method of claim 10, wherein the electronic device comprises a package substrate.

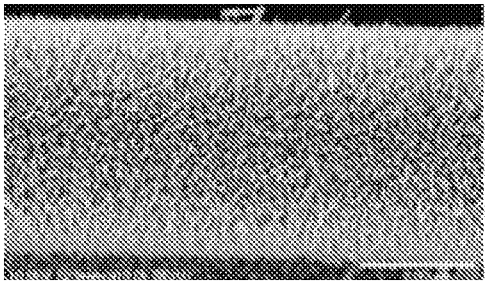


Fig. 1A (prior art)

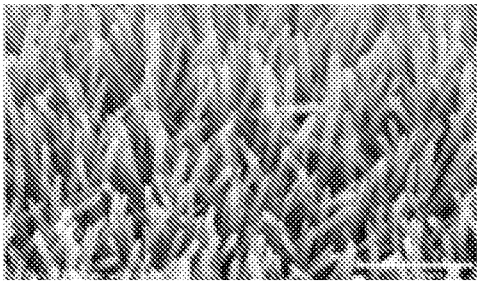


Fig. 1B (prior art)

Fig. 2

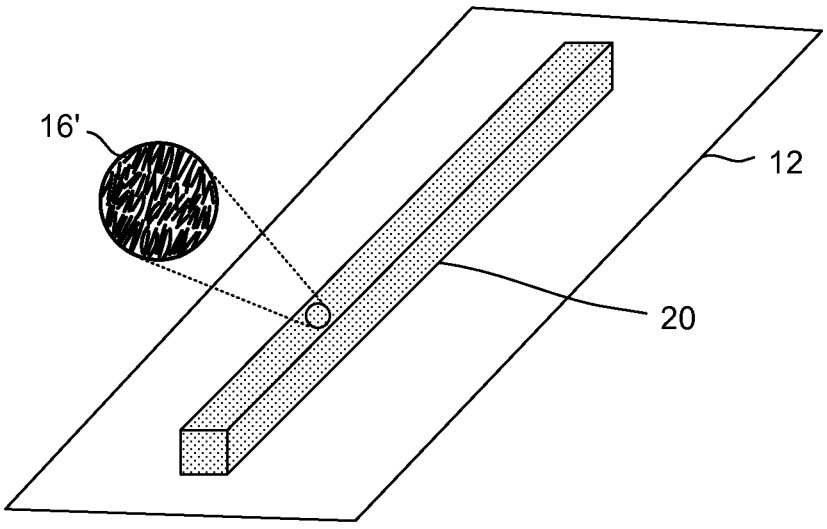


Fig. 3A

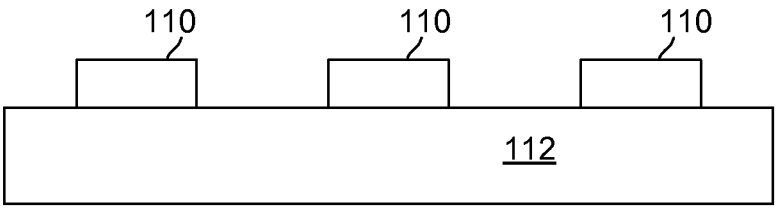


Fig. 3B

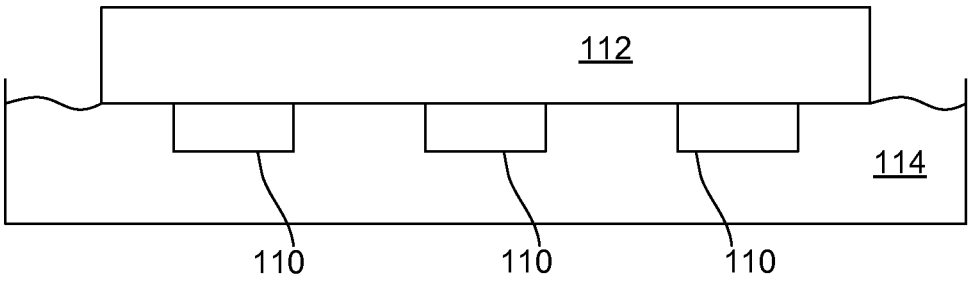


Fig. 3C

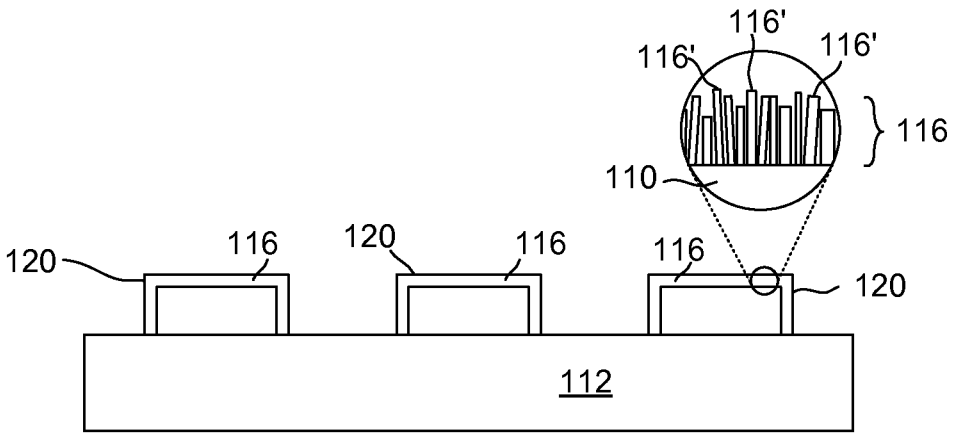


Fig. 3D

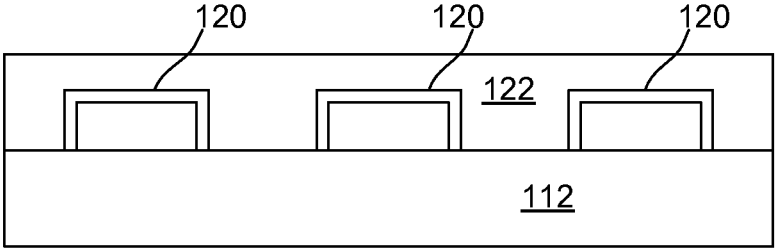


Fig. 4

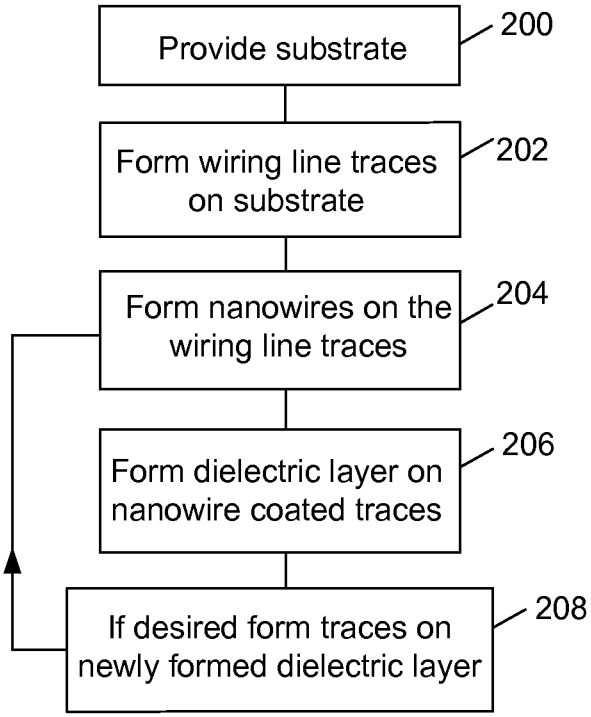
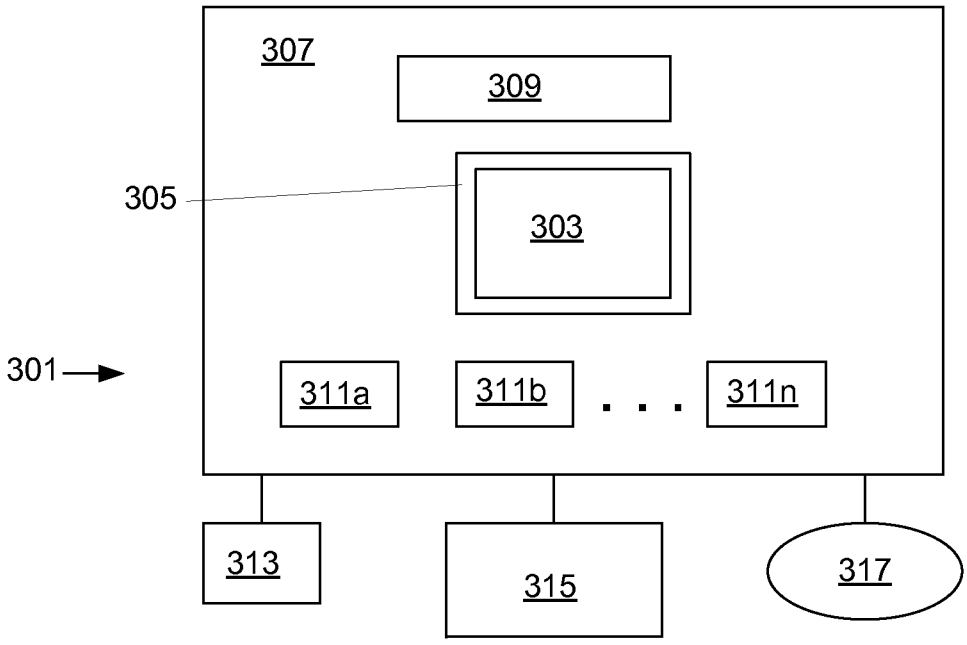

Provide substrate
200
Form wiring line traces on substrate
202
Form nanowires on the wiring line traces
204
Form dielectric layer on nanowire coated traces
206
If desired form traces on newly formed dielectric layer
208

Fig. 5


307
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311a
311b
311n
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317

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2011/067261

A. CLASSIFICATION OF SUBJECT MATTER

HOIL 21/28(2006.01)i, B82B 3/00(2006.01)1

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

HOIL 21/28; HOIL 21/302; HOIL 21/768; HOIL 23/34; HOIL 23/48; B32B 27/06; B32B 3/10; HOIL 21/461

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: nanowire, copper, dielectric layer, and metal trace

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y A	US 2010-0028633 Al (CT R0URKE SHAWN et al.) 04 February 2010 See the abstract, figure 1, paragraphs [0026]-[0036] and claim 1.	1-2, 6-7 3-5, 8-16, 18-20 17
Y	US 6762494 Bl (FAZELP0UR; SIAMAK et al.) 13 July 2004 See the abstract, figure 3, columns 3-4 and claim 1.	3-5, 8-16, 18-20
Y	US 2003-0126742 Al (JYH-MING TING et al.) 10 July 2003 See the abstract, figure 1, paragraphs [0028]-[0036] and claim 1.	12-15, 18
A	US 2010-0207269 Al (KRUGLICK EZEKIEL) 19 August 2010 See the abstract, figures 1-2, pages 1-3 and claims 1-12.	1-20

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
17 SEPTEMBER 2012 (17.09.2012)	**19 SEPTEMBER 2012 (19.09.2012)**

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Authorized officer

K[i]m, Sang-Taek

Telephone No. 82-42-481-8623

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US201 1/067261

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